High-Speed, Spurious-Free Sequential Phase Frequency Detector and Dual-Modulus Prescalers for RF Frequency Synthesis

Mathilde Sié [1,3], Gilles Cibiel [1], Éric Tournier [1,2], Robert Plana [1,2] and Jacques Graffeuil [1,2]

LAAS-CNRS [1] and University Paul Sabatier [2], 7 avenue du Colonel Roche, 31077 Toulouse, France
STMicroelectronics SA [3], 850 rue Monnet, 38926 Crolles, France

Abstract — **Original integrated 22-GHz dual-modulus static frequency dividers (4/5) realized in a Silicon Germanium BiCMOS technology dedicated for high volume production are presented. They operate at low bias voltage (3.3 V) and provide balanced output signals on 50 ohm loads. An optimized digital tri-state phase/frequency detector (PFD) is also reported. A new proposed architecture and original logic approach translate into excellent spurious immunity and high-speed detection: the proposed structure has the advantage to cancel the spurious which are present whatever the state of the comparator. Such features make these versatile circuits blocks essential for low noise, high-frequency PLL systems.**

I. Introduction

Frequency synthesizers are common elements in modern electronic systems: their maximum operating frequency and spectral purity are often critical to system performance. Most synthesizers are of the phase-locked type, employing a digital frequency divider, that makes possible the comparison of the divided output with respect to the input reference, and a digital phase/frequency detector, easy to integrate monolithically, which allows wide-band frequency operation. In a first part, we report the originalities of our digital dual-modulus dividers structures compared to the existing ones: the ECL logic and the schematic modifications that have been implemented turn to frequency performances which are, at present, at the state of the art for a 0.25 µm technology [1, 2]. These prescalers will be subsequently used to design a programmable divider with a selectable division ratio which is composed by a divider $N / N + 1$ and two CMOS counters. In the second part, we present a new structure of digital tri-state comparator which the noise contribution is very low in comparison with other classical digital detectors. We will explain in detail the presence and the consequence of voltage spurious in the tri-state comparator operation. Our goal consists of annihilation of these spurious on detector's outputs.

In general, our findings lead for the optimization of digital circuits which take place in PLL [3].

II. Dual-Modulus Frequency Divider Design

The dual-modulus prescalers $N / N + 1$ are generally designed from a synchronous structure [4], i.e. each circuit evolution is dependent upon the same clock rising edge. The division by $N = 4$ is then obtained by a Johnson cell: two dividers by 2 connected in series and operated synchronously. The division by $N + 1 = 5$ is realized by the masking of the divide by 4's output signal during one clock's period in order to freeze the circuit evolution during this time. The problem with this kind of structure is on the return loop: the divider by 4's output signal has to propagate through the input masking NAND gate in a time less than one clock period in order to trigger the first D flip-flop before the next clock rising edge. As soon as the frequency exceeds a given value, this signal needs more than one clock period to propagate through this "critical path" (i.e. return loop), and the dual modulus prescaler does no longer achieve the dividing process.

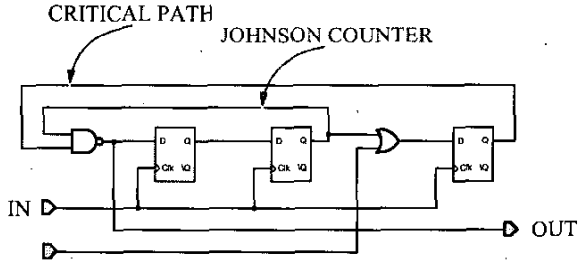

Figure 1: Classical prescaler $N / N + 1$ topology

To get rid of this frequency limitation, we suggest the use of an asynchronous logic as shown in the schematics of Figures 2 and 4: the division by 4 is realized by an asynchronous connection of two dividers by 2. Concerning the division by $N = 5$, the circuit of Figure 2 presents a novelty: the division factor $N + 1$ is obtained by masking the clock signal, on a path which is less critical than in the classical solution [5].

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This prescaler has been processed using the BiCMOS7 0.25 µm STMicroelectronics technology (cf. Fig.6) and measured: its bias voltage is 3.3 V and its consumption is about 70 mW.

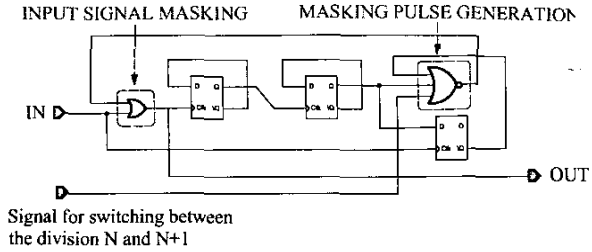

Figure 2: First original $N/N+1$ prescaler topology

It must be enlightened that, first, the maximum measured operating frequency of the 4/5 divider is 22 GHz. We must emphasize that this dual-modulus prescaler is the first stage of a programmable divider with a selectable ratio: so, if the dual-modulus prescaler which manages the highest frequencies is able to operate up to 22 GHz, the full divider will have the same frequency performances.

Figure 3 shows the input sensitivity and the available output power versus the input frequency. Because of the digital structure, there is no conversion loss: once the divider synchronized, the output power is unrelated to the input power. It must be understood that several dividers of the same kind can be cascaded together if the output power operating range is included in the input one. It can be seen in Figure 3 that this condition is fulfilled up to 20 GHz.

The output frequency spectrum of the first $N/N+1$ prescaler (Fig. 2) (for the $N+1$ ratio) at an input frequency of 20 GHz is shown in Figure 4 (for the $N+1$ ratio).

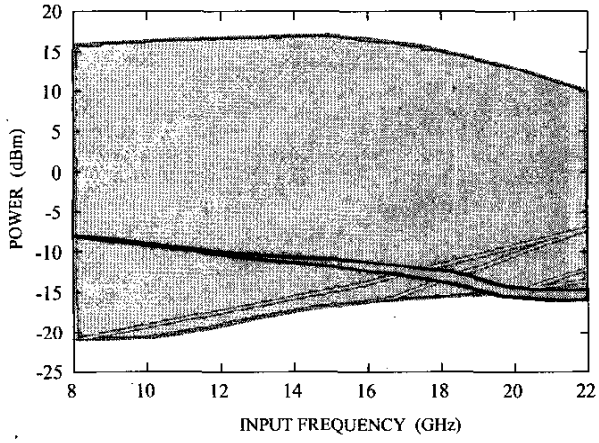

Figure 3: Measured input sensitivity (light gray) and available output power (dark gray)

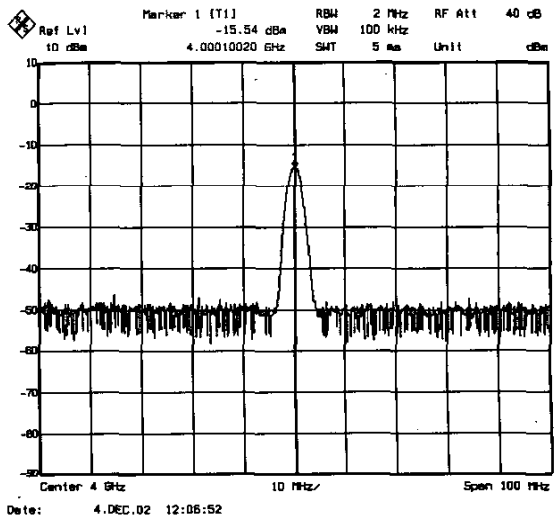

Figure 4: $N/N+1$ prescaler spectrum ($N=4$)

The computed additive phase noise of the first divider-by-2 from the $N/N+1$ prescaler is shown in Figure 5: it is comparable with the last published results [1].

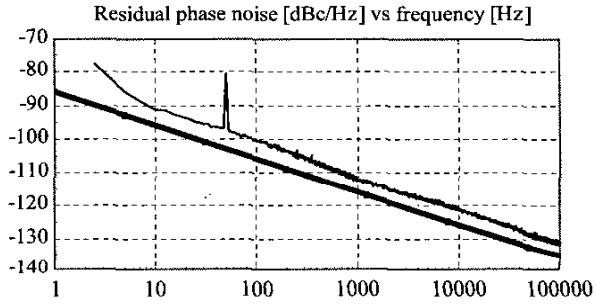

Figure 5: Phase noise simulation and measure of the divide by 2

However, a disadvantage remains, which prevents the divider from operating at very high frequencies: the clock signal has to propagate through the input OR gate and this gate has to accommodate the highest frequency signal. The drawback is that this gate, designed in ECL logic like all the dual-modulus prescaler, is based on a dissymmetric differential pair which cannot accommodate high frequencies. Therefore, to avoid this problem, the OR gate is replaced by a D-Latch (cf. Fig. 7). In fact, the D-Latch structure is perfectly symmetric both in the layout and in its operation, and will exhibit an enhanced maximum operating frequency.

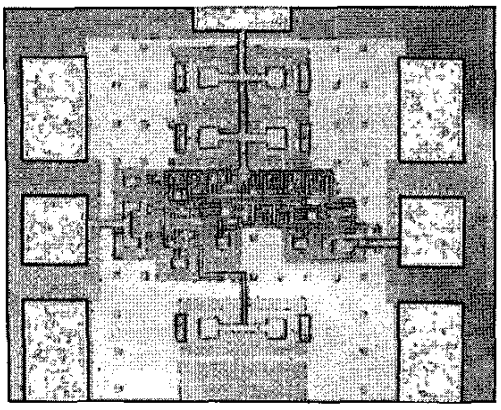

Figure 6: First $N / N+1$ prescaler microphotograph (240 µm × 295 µm)

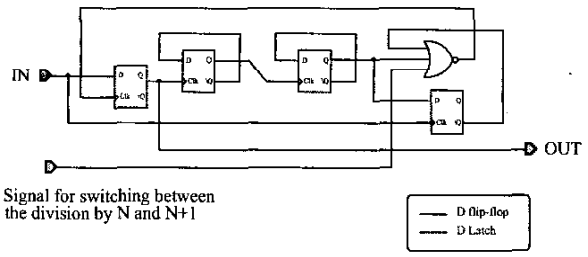

Figure 7: Second original $N / N+1$ prescaler topology

III. Digital Tri-State PFD Design

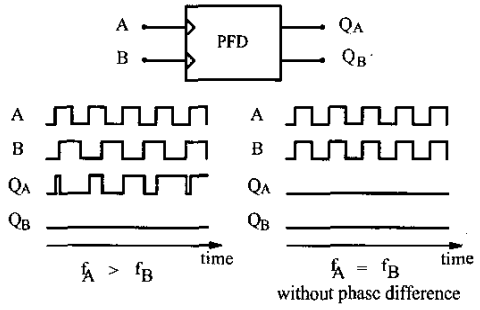

Figure 8: Ideal operating sequential PFD

Sequential phase/frequency detectors (PFDs) which already exist today (cf. Fig. 9) are based on a recurrent topology [3,6]: this circuit, that add frequency detection to the phase one, proves its extremely usefulness because it significantly increases the acquisition range and lock speed of PLLs.

Unlike multipliers and XORs, digital tri-state comparators generate two outputs that are not complementary. Illustrated in Figure 8, the operation of a typical PFD is as follows. If the frequency of input A is greater than that of input B, then the PFD produces positive pulses at Q_A, while Q_B remains at zero. Conversely, if $\omega_A < \omega_B$, then positive pulses appear at Q_B while $Q_A = 0$. If $\omega_A = \omega_B$, then the circuit generates pulses at either Q_A and Q_B with a width equal to the phase difference between the two inputs. Note that, in principle, Q_A and Q_B are never high simultaneously.

Thus, the average value of $(Q_A - Q_B)$ is an indication of the frequency or phase difference between A and B. The outputs Q_A and Q_B are usually called the "UP" and "DOWN" signals.

However, this structure presents the following drawback: it is designed in CMOS logic. This logic firstly operates more slowly than the ECL one and secondly involves the use of high amplitude signals (3.3 V) which generate a higher noise in the loop. In addition to these drawbacks, RESET pulses or "spurious", absent in the ideal operating principle, exist in fact when the PFD operates, and are a source of noise in the loop (cf. Fig. 9).

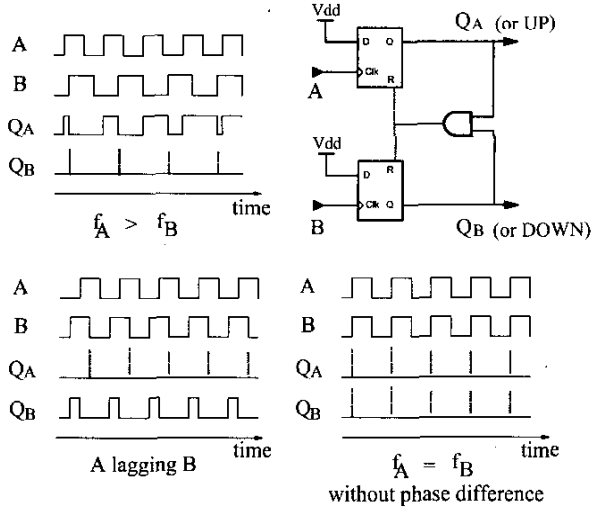

Figure 9: Real operating sequential PFD

To prevent these defects, we propose firstly to use the ECL logic to design a PFD which operates in a wide frequency bandwidth (1 to 20 GHz) and has a weak voltage excursion to reduce noise generation in the loop. Moreover, in order to eliminate the RESET pulses, the classic digital PFD schematic has been modified: the simplified structure presented in Figure 10 enables the cancellation of the spurious on the outputs UP and DOWN.

To carry out the cancellation of the PFD outputs signals, we use the RESET pulses (produced by the AND gate) that trigger two complex XOR gates in ECL logic. Two non-inverter gates, placed on the one of the XOR gate inputs, are used to compensate for the time delay when the signal propagates through the AND gate. A classic PFD in ECL logic has already been processed (cf. Fig. 11) and the design of the proposed novel topology is near for completion (cf. Fig. 10).

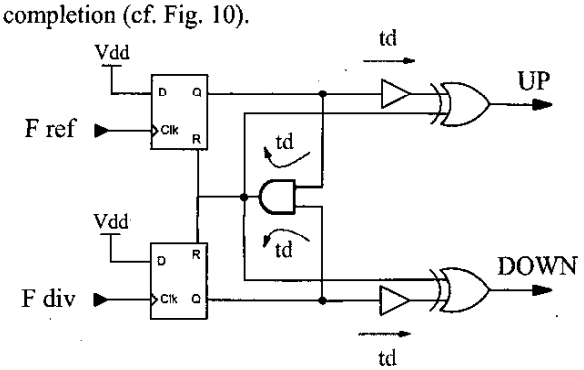

Figure 10: Simplified logic scheme of the novel digital tri-state comparator

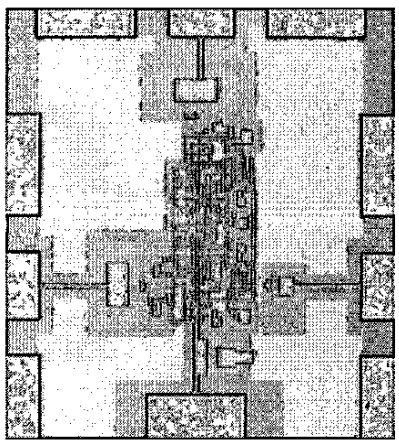

Figure 11: Classic ECL PFD layout (445 µm × 475 µm)

The open-loop characterization of the circuit composed by the PFD (cf. Fig. 11), a charge pump and a filter is not trivial, because of the signal integration required by the frequency detection. A complete symmetry of current sinking and sourcing in the filter by the charge pump is impossible, due to mismatch in components. Then, it is not possible to maintain the output voltage away from the supply bounds to make measurements, because the non-null mean of the current flowing into the filter always implies a deviation of the output voltage. Only a closed loop can be used to achieve the output voltage control. We design at present a PLL using fully characterized VCO, divider and filter in order to deduct the PFDs performances.

IV. Conclusion

In this paper, we have proposed novel topologies of digital functions which take place a part in frequency PLL systems. Original frequency dual-modulus prescalers and a novel sequential phase/frequency detector were designed and fabricated in a 0.25 µm SiGe technology intended for high volume production. The original chosen architecture, the dedicated design approach and the BiCMOS SiGe process capabilities led to a good trade-off between maximum input frequency, input sensitivity, noise floor, power consumption, division ratios and die size compared with the current available high-frequency dividers and classical high-frequency PFD.

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